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FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 98-P-104D1 (850063.542D1)	APPLICATION NO. 10/827,409
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Robert Louis Hodges	
		FILING DATE April 19, 2004	GROUP ART UNIT 2822

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,378,627	04/05/83	Jambotkar	~~29~~ 438	~~57~~ 291	
	AB	4,419,810	12/13/83	Riseman	~~29~~ 438	~~57~~ 303	
	AC	4,758,528	07/19/88	Goth et al.	~~437~~ 438	~~15~~ 514	
	AD	5,027,185	06/25/01	Liauh	~~357~~ 257	~~59~~ 413	
	AE	5,434,093	07/18/95	Chau et al.	~~437~~ 438	~~41~~ 300	
	AF	5,597,752	01/28/97	Niwa	~~437~~ 438	~~44~~ 291	
	AG	5,637,516	06/10/97	Müller	438	203	
	AH	5,688,700	11/18/97	Kao et al.	~~437~~ 438	~~29~~ 289	
	AI	5,796,157	08/18/98	Fallico et al.	257	557	
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	~~AK~~					
	AL					
	AM					
	AN					
	AO					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AP	IBM Technical Disclosure Bulletin, Vol. 28 #7 pp. 2767-2768, 12/85, 257/346
	AQ	IBM Technical Disclosure Bulletin, Vol. 31 #7 pp. 311-312, 12/88, 257/346
	AR	Wolf et al., "Silicon Processing for the VLSI", Volume 1, Pages 191-194, 1986.

EXAMINER John M. Smith DATE CONSIDERED 11/16/05

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).